



**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

**In re Application of:** James M. Derderian

**Serial No.:** 09/938,106

**Filed:** August 23, 2001

**For:** ASSEMBLIES INCLUDING  
STACKED SEMICONDUCTOR DEVICES  
SEPARATED BY DISCRETE  
CONDUCTIVE ELEMENTS  
THEREBETWEEN, PACKAGES  
INCLUDING THE ASSEMBLIES, AND  
METHODS

**Confirmation No.:** 1038

**Examiner:** J. Im

**Group Art Unit:** 2811

**Attorney Docket No.:** 2269-4832US

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**APPEAL BRIEF**

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Attn: Board of Patent Appeals and Interferences

Sirs:

This APPEAL BRIEF is being submitted in the format required by 37 C.F.R.  
§ 41.37(c)(1), with the fee required by 37 C.F.R. § 41.20(b)(2).

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I. REAL PARTY IN INTEREST

U.S. Application Serial No. 09/938,106 (hereinafter “the ‘106 Application”), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc., as evidenced by the assignment that has been recorded with the U.S. Patent & Trademark Office (hereinafter “the Office”) at Reel No. 012120, Frame No. 0618. Accordingly, Micron Technology, Inc., is the real party in interest in the above-referenced appeal.

II. RELATED APPEALS AND INTERFERENCES

The final rejections of the claims in the divisional of the above-referenced application, U.S. Application Serial No. 10/230,452, filed August 29, 2002, are currently the subject of an appeal before the Board of Patent Appeals and Interferences and may affect the Board’s decision in the above-referenced appeal.

Neither Appellants nor their attorneys of record are aware of any other appeals, interferences, or other proceedings that would affect the Board’s decision in the above-referenced appeal.

III. STATUS OF CLAIMS

The ‘106 Application was filed with sixty-nine (69) claims on August 23, 2001.

Claims 1-22, 36-39, 52, and 65-69 were withdrawn from consideration following restriction and species election requirements.

Claims 1-22, 28, and 65-69 have been canceled without prejudice or disclaimer.

Claims 23-27 and 29-64 remain pending in the above-referenced application.

Of these, the Office has only considered claims 23-27, 29-35, 40-51, and 53-64. Final rejections were presented against each of claims 23-27, 29-35, 40-51, and 53-64.

**IV. STATUS OF AMENDMENTS**

The '106 Application was filed on August 23, 2001, with sixty-nine (69) claims.

The Examiner issued restriction and species election requirements in an action dated August 1, 2002. A response was mailed on September 1, 2002, and received a filing date of September 3, 2002.

On November 21, 2002, a first action on the merits was mailed. That action indicated that claims 1-22, 36-39, 52, and 65-69 had been withdrawn from consideration. Each of the claims which had been considered, including claims 23-35, 40-51, and 53-64, stood rejected. In response, an amendment was mailed on February 21, 2003, and received a filing date of February 23, 2003. In that Amendment, claim 28 was canceled without prejudice or disclaimer and claims 23, 26, 27, 41, 44, 45, and 48 were amended. In addition, explanations as to the patentability of claims 23-35, 40-51, and 53-64 were provided.

Evidently, the explanations that were provided in the Amendment of February 23, 2003, were somewhat convincing, as entirely new grounds for rejecting the claims were set forth in a Final Office Action dated May 22, 2003. The new grounds of rejection were addressed in an Amendment Under 37 C.F.R. § 1.116 dated July 14, 2003. Revisions to claims 23 and 45 (second amendment) were presented in that Amendment, as was reasoning demonstrating the patentability of the claims over the art upon which the rejections were based.

On August 6, 2003, an Advisory Action was mailed. The Advisory Action indicated the Examiner's unwillingness to consider the claim revisions that had been presented in the Amendment Under 37 C.F.R. § 1.116 because the revisions purportedly required an additional search. In order to facilitate entry of the claim revisions, a Request for Continued Examination (RCE) was filed on August 11, 2003.

Another non-final action on the merits was issued on November 6, 2003. In that action, new rejections were presented against claims 23-35, 40-51, and 53-64. On February 5, 2004, an Amendment was filed in response to the Office Action of November 6, 2003. Claims 1-22 and 65-69, which were withdrawn from consideration pursuant to the restriction requirement of August 1, 2002, were canceled without prejudice or disclaimer. In addition, revisions were presented to each of the claims that remained pending. The Amendment was accompanied by remarks explaining the patentability of the claims that remained pending.

In a Final Office Action dated May 6, 2004, the Examiner maintained several of the rejections that had been previously asserted against the claims. Further remarks showing the patentability of the claims over the art of record were presented in a Response to Final Office Action, which was mailed on July 6, 2004.

The Examiner again rejected Appellant's reasoning, as evidenced by the comments that accompanied the Advisory Action dated August 5, 2004. On September 7, 2004, another RCE was filed along with an Amendment, in which claims 23 and 45 were again amended to recite the same subject matter in a manner that was hoped to be better understood by the Examiner. No further amendments to the claims have been presented in the above-referenced application.

Despite careful explanations as to the patentability of the pending claims over the art upon which the Examiner's rejections have been based (*see* communications from Appellants dated September 7, 2004, January 6, 2005, and June 6, 2005), the Examiner has continued to maintain rejections that were originally presented in the Office Action of November 6, 2003 (*see* Office Actions of October 6, 2004, April 5, 2005, and Advisory Action of June 21, 2005).

In view of the Examiner's continued rejection of the claims, a Notice of Appeal was filed on June 24, 2005.

This APPEAL BRIEF follows the Notice of Appeal, is being submitted with a one-month petition for extension of time and the appropriate fee, and should be deemed to have been submitted within three months of the mailing date of the Notice of Appeal, as September 24, 2005, fell on a Saturday. 37 C.F.R. § 1.7.

#### V. SUMMARY OF CLAIMED SUBJECT MATTER

The '106 Application includes claims that are directed to methods for assembling semiconductor devices. Such an assembly method includes providing a first semiconductor device. Paragraph [0012]; Figs. 8, 15, 18. Discrete conductive elements are placed over portions of an active surface of the first semiconductor device. *Id.* Alternatively, a first semiconductor device with pre-positioned discrete conductive elements may be provided. A second semiconductor device is positioned at least partially over the first semiconductor device, and rests upon the discrete conductive elements in electrical isolation therefrom. *Id.* The discrete conductive elements determine, at least in part, the distance the first and second semiconductor devices are spaced apart from one another. *Id.*; paragraph [0013]. Adhesive material, which may

be introduced between the first and second semiconductor devices to secure them to one another, may also affect the distance that the first and second semiconductor devices are spaced apart from each other. Paragraphs [0017], [0018], [0020].

VI. GROUND OF REJECTION TO BE REVIEWED ON APPEAL

(A) Whether, under 35 U.S.C. § 102(e), the subject matter recited in claims 23, 24, 29, 30, 33, 40, 45, 46, 49, 50, 53, 59, and 61-64 is novel and, thus, patentable over the subject matter described in U.S. Patent 6,400,007 to Wu et al. (hereinafter “Wu”);

(B) Whether, under 35 U.S.C. § 103(a), claims 25, 26, 31, 34, 35, 41-44, 47, 51, 54-58, and 60 are drawn to subject matter that is non-obvious and, thus, patentable over the subject matter taught in Wu, in view of teachings from U.S. Patent 6,388,313 to Lee et al. (hereinafter “Lee”); and

(C) Whether, under 35 U.S.C. § 103(a), the subject matter to which claims 27, 32, and 48 are directed is allowable over the teachings of Wu, in view of teachings from U.S. Patent 6,531,784 to Shim et al. (hereinafter “Shim”).

VII. ARGUMENT

A. REJECTIONS UNDER 35 U.S.C. § 102

1. APPLICABLE LAW

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053

(Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

With respect to inherency, M.P.E.P. § 2112 provides:

The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) . . . ‘To establish inherency, the extrinsic evidence ‘must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill . . .’ *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1991) (emphasis supplied).

## 2. REFERENCE RELIED UPON

### *Wu*

The description of Wu is limited to a method for supporting an upper, or second, semiconductor die 34 over a first semiconductor die 28 with an adhered glue layer 50 or a feature that is identified in the drawings as element “54.” More specifically, Wu describes stacked semiconductor device assemblies, as well as assembly methods. An assembly according to Wu, shown in FIG. 4 thereof, includes a substrate 26. *See also* col. 3, lines 15-18. A first semiconductor die 28 secured to the substrate 26 with glue 30, 50. *See* FIG. 4; col. 3, lines 15-18. A projecting element 52, such as a dam, protrudes from substrate 26 and causes the glue 50 that secures first semiconductor die 28 to substrate 26 to extend upwardly around the outer periphery of the first semiconductor die 28 and to a location beyond the plane in which the active surface 46 of the first semiconductor die 28 is located. Col. 3, lines 18-26.

Wires 32 electrically connect bonding pads 48 of the first semiconductor die 28 to corresponding signal input terminals 40 of the substrate 26. Col. 3, lines 30-32. An element

identified in FIGs. 3 and 4 of Wu as “54” is positioned on the active surface 46 of the first semiconductor die 28, between two rows of bonding pads 48. *See also* col. 3, lines 36-40.

Element “54” appears to support a second semiconductor die 34, which is positioned over the first semiconductor die 28. *See* FIGs. 3 and 4.

In assembling these components, glue 30 is applied to a surface of the substrate 26, within the confines of the projecting element 52, or dam. Col. 3, lines 18-26. A backside of the first semiconductor die 28 is brought into contact with the glue 30. Col. 3, lines 15-18. As the first semiconductor die 28 is biased toward the substrate 26, the glue 30 oozes upwardly, around the peripheral edges of the first semiconductor die 28, and onto peripheral portions of the active surface 46 thereof to form an adhered glue layer 50. Col. 3, lines 18-26. Next, wires 32 are formed between bonding pads 48 of the first semiconductor die 28 and corresponding signal input terminals 40 of the substrate 26. Col. 3, lines 30-32.

Thereafter, element “54” is placed on the active surface 46 of the first semiconductor die 28. Only after element “54” and adhered glue layer 50 are in place is the second semiconductor die 34 positioned over the first semiconductor die 28 and on element “54.” *See* FIGs. 3 and 4.

### 3. ANALYSIS

Claims 23, 24, 29, 30, 33, 40, 45, 46, 49, 50, 53, 59, and 61-64 have been rejected under 35 U.S.C. § 102(e) for reciting subject matter which is purportedly anticipated by that described in Wu.

It is apparent that the Examiner did not focus on the subject matter recited in claims 23, 24, 29, 30, 33, 40, 45, 46, 49, 50, 53, 59, and 61-64. Instead, it appears that the Examiner focused on the subject matter disclosed in the specification of the above-referenced application.

Independent claim 23 recites, among other things, “positioning a second semiconductor device at least partially over [a] first semiconductor device, a back side of the second semiconductor device *resting upon at least some . . . discrete conductive elements and being supported thereby . . .*” (emphasis supplied). Independent claim 45 recites, among other things, “positioning a second semiconductor device at least partially over [a] first semiconductor device and on at least some discrete conductive elements . . . such that *the second semiconductor device is supported by the at least some discrete conductive elements . . .*” Neither independent claim 23 nor independent claim 45 requires that anything other than discrete conductive elements support a second semiconductor device.

It has been asserted, at pages 2 and 3 of the Final Office Action of April 5, 2005, that FIG. 5 of Wu shows wires 32 supporting the second semiconductor die 34. The figures of Wu can only be relied upon for what they reasonably show, based on the specification of Wu. M.P.E.P. § 2125. FIG. 5 of Wu does not clearly depict any of the features located between the first semiconductor die 28 and the second semiconductor die 34. Moreover, the figures of Wu could not be considered to definitively show whether element 54, the adhered glue 50, the wires 32, or some combination thereof supports the second semiconductor die 34.

When viewed in the context of the specification of Wu, it is clear that the second semiconductor die 34 “is stacked above” the first semiconductor die 28 “by adhered glue 50,”

indicating that the adhered glue 50 supports the second semiconductor die 34. Col. 3, lines 36-40.

As the specification of Wu provides no further detail, and the delicate wires 32 do not necessarily support the second semiconductor die 34, Wu does not expressly or inherently describe that the “a back side of the second semiconductor [die 34] rest[s] upon at least some of the [wires 32]” or that “the second semiconductor [die 34] is supported by . . . at least some discrete conductive elements,” as would be required to uphold the 35 U.S.C. § 102(e) anticipation rejections of independent claims 23 and 45, respectively.

Claims 24, 29, 30, 33, and 40 are each allowable, among other reasons, for depending either directly or indirectly from claim 23, which is allowable.

Claim 24 is further allowable because Wu lacks any express or inherent description of positioning a second semiconductor die 34 over wires 32 with a back side of the semiconductor die 34 and wires 32 “in mutual electrical isolation.” Instead, the disclosure of Wu is focused on preventing short circuiting between wires 32 and an active surface of the first semiconductor die 28, over which wires 32 extend.

Claim 30 is additionally allowable since Wu does not expressly or inherently describe “drawing” second semiconductor die 34 thereof toward first semiconductor die 28. Instead, the description of Wu is limited to “stack[ing]” second semiconductor die 34 above first semiconductor die 28. As evidenced by the disclosures of U.S. Patents 4,891,436 and 6,156,146, copies of which were previously provided to the Office, resins and other adhesive materials do not necessarily shrink when cured. They may instead expand. Furthermore, Wu is silent as to whether adhered glue 50 is in a cured or uncured state when second semiconductor die 34 is

positioned over adhered glue 50. As adhered glue 50 does not necessarily shrink when cured and since adhered glue 50 is not necessarily in an uncured state when second semiconductor die 34 is positioned thereover, Wu does not inherently describe each and every element of claim 30.

Claim 33 is also allowable since Wu includes no express or inherent description that a quantity of adhesive material (adhered glue 50 or element 54) is applied to an active surface of first semiconductor die 28 “after . . . positioning the second semiconductor” die 34 thereover. Instead, Wu clearly discloses that adhered glue 50 is applied to first semiconductor die 28 before second semiconductor die 34 is positioned thereover. Col. 3, lines 36-40.

Each of claims 46, 49, 50, 53, 59, and 61-64 is allowable, among other reasons, for depending either directly or indirectly from claim 45, which is allowable.

Claim 50 is additionally allowable since Wu does not expressly or inherently describe “drawing” second semiconductor die 34 thereof toward first semiconductor die 28. Instead, the description of Wu is limited to “stack[ing]” second semiconductor die 34 above first semiconductor die 28. As evidenced by the disclosures of U.S. Patents 4,891,436 and 6,156,146, resins and other adhesive materials do not necessarily shrink when cured. They may instead expand. Furthermore, Wu is silent as to whether adhered glue 50 is in a cured or uncured state when second semiconductor die 34 is positioned over adhered glue 50. As adhered glue 50 does not necessarily shrink when cured and since adhered glue 50 is not necessarily in an uncured state when second semiconductor die 34 is positioned thereover, Wu does not inherently describe each and every element of claim 50.

Claim 53 is also allowable since Wu includes no express or inherent description that a quantity of adhesive material (adhered glue 50 or element 54) is applied to an active surface of first semiconductor die 28 “after . . . positioning the second semiconductor” die 34 thereover. Instead, Wu clearly discloses that adhered glue 50 is applied to first semiconductor die 28 before second semiconductor die 34 is positioned thereover. Col. 3, lines 36-40.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 23, 24, 29, 30, 33, 40, 45, 46, 49, 50, 53, 59, and 61-64 be reversed.

B. REJECTIONS UNDER 35 U.S.C. § 103(a)

1. APPLICABLE LAW

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant’s disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

2. ADDITIONAL REFERENCE RELIED UPON

*Lee*

Lee teaches a process for forming a multi-chip module. That process includes, among other things, securing a first semiconductor chip 21 to a substrate 20. FIG. 1; col. 5, lines 5-7. Bond pads 210 of first semiconductor chip 21 are electrically connected to corresponding terminals (not shown) of substrate 20 by bond wires 22. FIG. 1; col. 5, lines 7-10. A so-called “reverse wire-bonding technique” is employed so as to minimize the distance that bond wires 22 protrude above the active surface of first semiconductor chip 21. Col. 5, lines 10-21. Next, an electrically insulative adhesive layer 23 is applied over first semiconductor chip 21. FIG. 1; col. 5, lines 22-25. The adhesive layer 23 completely surrounds bond wires 22 (FIG. 1; col. 5, lines 22-32, 41-49, and 50-59) in such a way as to prevent the bond wires 22 from contacting the nonactive surface of a second semiconductor chip 24 (col. 3, lines 37-42). The second semiconductor chip 24 is then positioned over first semiconductor chip 21 and secured thereto by way of adhesive layer 23. *Id.* Lee teaches that the adhesive layer 23 and the underlying first semiconductor chip 21 support the second semiconductor chip 24. Col. 6, lines 5-13, 25-29.

3. ANALYSIS

a. WU IN VIEW OF LEE

Claims 25, 26, 31, 34, 35, 41-44, 47, 51, 54-58, and 60 have been rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over the subject matter taught in Wu, in view of teachings from Lee.

Claims 25, 26, 31, 34, 35, and 41-44 are each allowable, among other reasons, for depending indirectly from claim 23, which is allowable.

Each of claims 47, 51, 54-58, and 60 is allowable, among other reasons, for depending indirectly from claim 45, which is allowable.

i. NO MOTIVATION TO COMBINE

It is also respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 25, 26, 31, 34, 35, 41-44, 47, 51, 54-58, or 60 because one of ordinary skill in the art would not have been motivated to combine the teachings of Wu and Lee in the manner that has been asserted. In particular, neither Wu nor Lee teaches or suggests that a back side of an upper semiconductor device may be supported by bond wires or other intermediate conductive elements extending over the active surface of a lower, adjacent semiconductor device.

ii. NO EXPECTATION OF SUCCESS

It is further submitted that one of ordinary skill in the art would have had no reason to expect the asserted combination of teachings from Wu and Lee to be successful. Again, as neither of these references teaches or suggests that bond wires may support an upper semiconductor device, there would be no reason for one of ordinary skill in the art to expect that teachings from Wu and Lee could be combined in such a way as to render the subject matter of any of claims 25, 26, 31, 34, 35, 41-44, 47, 51, 54-58, and 60 obvious under 35 U.S.C. § 103(a).

Rather, it appears that the Examiner's obviousness rejection of these claims was based solely and improperly upon the hindsight provided by the subject matter disclosed and claimed in the above-referenced application.

iii. THE REFERENCES DO NOT TEACH OR SUGGEST EACH AND EVERY ELEMENT OF SEVERAL CLAIMS

It is further submitted that Wu and Lee, taken either together or separately, do not teach or suggest each and every element of several of the rejected claims, as is required to establish a *prima facie* case of obviousness.

Claim 31 is allowable since Wu and Lee both lack any teaching or suggestion that the adhesive materials or resins disclosed therein are capable of drawing two semiconductor devices toward one another "by at least one of capillary action . . . , curing . . . , application of heat . . . , and vibration." While Wu and Lee both teach use of adhesive layers to secure adjacent elements, neither Wu nor Lee teaches or suggests an adhesive layer that is capable of drawing two elements toward one another.

Claim 34 is allowable because neither Wu nor Lee teaches or suggests that two semiconductor device may be drawn toward one another.

Claim 35, which depends from claim 34, is also allowable since Wu and Lee do not teach or suggest that curing of a glue, resin, or other adhesive material may cause two semiconductor devices to be drawn toward one another.

Claim 51 is allowable since both Wu and Lee lack any teaching or suggestion that the adhesive materials or resins disclosed therein are capable of drawing two semiconductor devices

toward one another “by at least one of capillary action . . . , curing . . . , application of heat . . . , and vibration.”

Claim 54 is allowable because neither Wu nor Lee teaches or suggests that two semiconductor device may be drawn toward one another.

Claim 55, which depends from claim 54, is also allowable since Wu and Lee do not teach or suggest that curing of a glue, resin, or other adhesive material may cause two semiconductor devices to be drawn toward one another.

Claim 57 is allowable because Wu and Lee both lack any teaching or suggestion of controlling biasing of one semiconductor device toward another.

Claim 58 is allowable since neither Wu nor Lee includes any teaching or suggestion of “controlling biasing force to a level insufficient to deform, kink, bend, or collapse . . . discrete conductive elements.” Wu actually teaches away from the subject matter recited in claim 58 by teaching the use of a projecting element 52 and overflow glue 58 to prevent shorting of wires 32 against first semiconductor die 28 as second semiconductor die 34 presses wires 32. Col. 3, lines 50-62.

b. WU IN VIEW OF SHIM

Claims 27, 32, and 48 are rejected under 35 U.S.C. § 103(a) for being directed to subject matter that is assertedly unpatentable over the teachings of Wu, in view of teachings from U.S. Patent 6,531,784 to Shim et al. (hereinafter “Shim”).

Claims 27 and 32 are both allowable, among other reasons, for depending indirectly from claim 23, which is allowable.

Claim 48 is allowable, among other reasons, for depending indirectly from claim 45, which is allowable.

Reversal of the 35 U.S.C. § 103(a) rejections of claims 25-27, 31, 32, 34, 35, 41-44, 47, 48, 51, 54-58, and 60 is respectfully requested.

C. ELECTION OF SPECIES REQUIREMENT

It is respectfully submitted that independent claims 23 and 45 remains generic to all of the species of invention of the second group that was identified in the Election of Species Requirement in the above-referenced application. In view of the allowability of these claims, claims 36-39 and 52, which have been withdrawn from consideration, should also be considered and allowed. M.P.E.P. § 806.04(d).

VIII. CLAIMS APPENDIX

The current status of each claim that has been introduced into the above-referenced application is set forth in CLAIMS APPENDIX to this Appeal Brief.

IX. EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132. Accordingly, no evidence appendix accompanies this Appeal Brief.

X. RELATED PROCEEDINGS APPENDIX

No decisions have been rendered by the Board or any court in a related application. Therefore, this Appeal Brief is not accompanied by a related proceedings appendix.

XI. CONCLUSION

(A) The subject matter recited in claims 23, 24, 29, 30, 33, 40, 45, 46, 49, 50, 53, 59, and 61-64 is novel and, thus, under 35 U.S.C. § 102(e), patentable over the subject matter described in Wu;

(B) Claims 25, 26, 31, 34, 35, 41-44, 47, 51, 54-58, and 60 are drawn to subject matter that is non-obvious and, thus, under 35 U.S.C. § 103(a), patentable over the subject matter taught in Wu, in view of teachings from Lee; and

(C) Under 35 U.S.C. § 103(a), the subject matter to which claims 27, 32, and 48 are directed is allowable over the teachings of Wu, in view of teachings from Shim.

Therefore, the rejections of claims 23-27, 29-35, 40-51, and 53-64 should be reversed. Additionally, claims 36-39 and 52 should be returned to consideration, and each of claims 23-27 and 29-64 should be allowed.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'Brick G. Power', with a long horizontal flourish extending to the right.

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Serial No. 09/938,106

## CLAIMS APPENDIX

23. A method for assembling semiconductor devices, comprising:  
providing a first semiconductor device;  
placing discrete conductive elements over portions of the first semiconductor device; and  
positioning a second semiconductor device at least partially over the first semiconductor device,  
a back side of the second semiconductor device resting upon at least some of the discrete  
conductive elements and being supported thereby, the back side and the at least some of  
the discrete conductive elements being electrically isolated from each other.
24. The method of claim 23, wherein the positioning the second semiconductor device  
comprises positioning the second semiconductor device on the at least some of the discrete  
conductive elements with the back side and the discrete conductive elements in mutual electrical  
isolation.
25. The method of claim 24, further comprising:  
providing a dielectric coating on at least portions of the discrete conductive elements.
26. The method of claim 25, wherein the providing comprises forming at least one of  
a dielectric oxide and a dielectric polymer coating on the at least portions of the discrete  
conductive elements.

27. The method of claim 24, wherein the positioning comprises positioning a dielectric layer on at least portions of the back side thereof.

29. The method of claim 23, further comprising:  
applying a quantity of adhesive material to at least an active surface of the first semiconductor device.

30. The method of claim 29, further comprising:  
drawing the second semiconductor device toward the first semiconductor device.

31. The method of claim 30, wherein the drawing is effected by at least one of capillary action of the adhesive material, curing of the adhesive material, application of heat to the adhesive material, and vibration of the adhesive material.

32. The method of claim 29, wherein the applying includes applying the quantity of adhesive material to the back side of the second semiconductor device.

33. The method of claim 29, wherein the applying is effected after the positioning the second semiconductor device.

34. The method of claim 33, further comprising:  
drawing the second semiconductor device toward the first semiconductor device.

35. The method of claim 34, wherein the drawing is effected during curing of the adhesive material.

36. The method of claim 29, wherein the applying is effected before the positioning the second semiconductor device.

37. The method of claim 36, further comprising:  
biasing at least one of the first and second semiconductor devices toward the other of the first and second semiconductor devices.

38. The method of claim 37, further comprising:  
controlling the biasing.

39. The method of claim 38, wherein the controlling the biasing comprises controlling biasing force to a level insufficient to deform, kink, bend, or collapse the discrete conductive elements.

40. The method of claim 23, further comprising:  
securing the first semiconductor device and a substrate to one another.

41. The method of claim 40, wherein the placing discrete conductive elements comprises securing the discrete conductive elements to contact areas of the substrate and bond pads of the first semiconductor device.

42. The method of claim 41, wherein the securing comprises electrically connecting bond pads of the second semiconductor device to corresponding contact areas of the substrate.

43. The method of claim 42, further comprising:  
encapsulating at least a portion of at least one of the substrate, the first semiconductor device,  
and the second semiconductor device.

44. The method of claim 42, further comprising:  
forming external conductive elements on the substrate in electrical communication with the  
corresponding contact areas.

45. A method for assembling semiconductor devices in a stacked arrangement with the stacked arrangement having a height substantially equal to combined thicknesses of each of the semiconductor devices and distances discrete conductive elements associated therewith protrude above the each of the semiconductor devices, comprising:  
providing a first semiconductor device with discrete conductive elements protruding from an active surface thereof; and

positioning a second semiconductor device at least partially over the first semiconductor device and on at least some discrete conductive elements of the discrete conductive elements such that the second semiconductor device is supported by the at least some discrete conductive elements and the back side and the at least some discrete conductive elements are electrically isolated from each other.

46. The method of claim 45, wherein the positioning comprises positioning the second semiconductor device on the at least some of the discrete conductive elements with a back side of the second semiconductor device electrically isolated from the discrete conductive elements.

47. The method of claim 46, further comprising:  
providing a dielectric coating on at least portions of the at least some of the discrete conductive elements.

48. The method of claim 46, wherein the positioning comprises positioning a second semiconductor device that includes a dielectric coating on at least portions of the back side thereof.

49. The method of claim 45, further comprising:  
applying a quantity of adhesive material at least to the active surface of the first semiconductor device.

50. The method of claim 49, further comprising:  
drawing the second semiconductor device toward the first semiconductor device.
51. The method of claim 50, wherein the drawing is effected by at least one of  
capillary action of the adhesive material, curing of the adhesive material, application of heat to  
the adhesive material, and vibration of the adhesive material.
52. The method of claim 49, wherein the applying is effected before the positioning.
53. The method of claim 49, wherein the applying is effected after the positioning.
54. The method of claim 53, further comprising:  
drawing the second semiconductor device toward the first semiconductor device.
55. The method of claim 54, wherein the drawing is effected during curing of the  
adhesive material.
56. The method of claim 49, further comprising:  
biasing at least one of the first and second semiconductor devices toward the other of the first and  
second semiconductor devices.

57. The method of claim 56, further comprising:  
controlling the biasing.

58. The method of claim 57, wherein the controlling the biasing comprises controlling biasing force to a level insufficient to deform, kink, bend, or collapse the discrete conductive elements.

59. The method of claim 45, further comprising:  
positioning the first semiconductor device relative to a substrate.

60. The method of claim 59, further comprising:  
connecting the discrete conductive elements to corresponding contact areas of the substrate.

61. The method of claim 59, further comprising:  
establishing electrical communication between bond pads of the second semiconductor device  
and corresponding contact areas of the substrate.

62. The method of claim 61, wherein the establishing communication comprises:  
placing additional discrete conductive elements between each of the bond pads and a  
corresponding contact area of the corresponding contact areas.

63. The method of claim 46, further comprising:  
providing at least one external connective element in communication with at least one bond pad  
of each of the first and second semiconductor devices.

64. The method of claim 63, further comprising:  
encapsulating at least portions of the first and second semiconductor devices.